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OPERATION AND MODELING OF THE MOS TRANSISTOR

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1.6 OVERVIEW OF THE MOS TRANSISTOR

1.6.1 Basic Structure

The basic idea on which the MOS transistor is based is over half a century old and is due to J. E. Lilienfeld, who obtained the first patents in the early 1930s[17]; see Fig. 1.19. Other patents were obtained by O. Heil.[18] Laboratory studies were performed in the late forties (see, for example, Ref. 19) but the device remained in the laboratory for over a decade following that. Then in the early sixties the MOS transistor "took off" following the demonstration of working devices by Kahng and Atalla,[20] the development of techniques for reliably growing oxides,[21] and the establishment of basic theories of operation.[22–25] A historical review of early work, including the development of practical fabrication techniques, can be found elsewhere.[26] Modern fabrication techniques are described in a number of books.[27–29]

We now offer a simple preview[30] of the MOS transistor, which will help introduce the detailed material in the rest of this book.

A simplified structure of an *n*-channel MOS transistor is shown in Fig. 1.20 (the names *n-channel* and MOS will be discussed shortly). The transistor is formed on a *p*-type silicon *body* (or *substrate*). Typical doping concentrations for the body are 10^{16} to 10^{18} cm^{-3}. The dopant concentration will be assumed uniform throughout the body, until further notice.

The center part of the structure is covered by an insulator (typically silicon dioxide, which is often referred to simply as *oxide*), usually of 35 to 100 Å thickness. The body interface to the oxide is often called the *surface*.

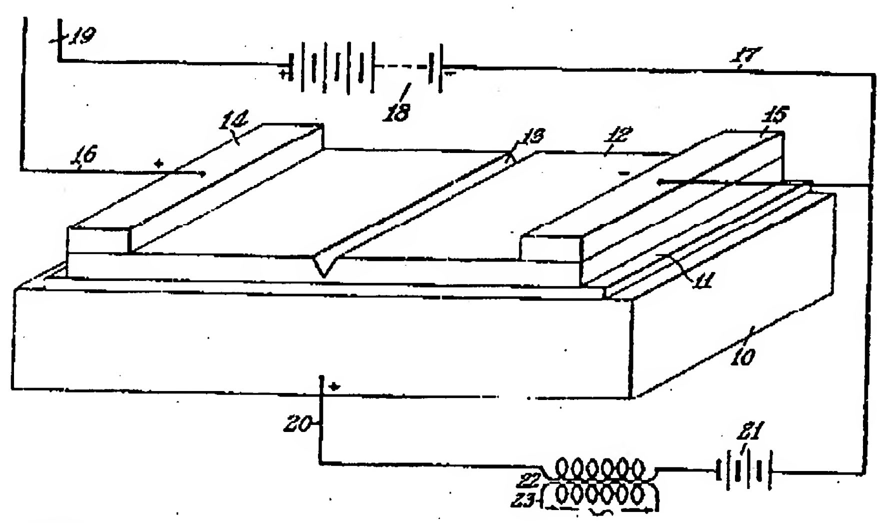

FIGURE 1.19
A figure from J. E. Lilienfeld's U.S. patent 1,900,018 (filed March 28, 1928; granted 1933). The structure should be turned upside down to correspond to the orientation used in this book (e.g., Fig. 1.20).

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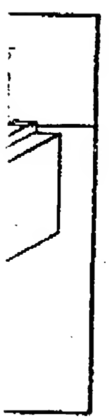

33) The struc-
Fig. 1.20).

A low-resistivity electrode, called the *gate*, is formed on top of the oxide. Contemporary processes commonly use polycrystalline silicon (*polysilicon*, or *poly*, for short) for the gate. This material, although silicon, is not a single crystal. Rather, it consists of many regions within each of which there is a regular array of atoms, and this regularity is broken at the boundaries between adjacent regions. The polysilicon material is heavily doped p or n type (e.g., 10^{20} cm^{-3}). The two regions shown on the sides are formed by implanting donor atoms, with the gate acting as a mask against the implant; this mask receives the donor atoms itself and prevents them from landing under it. Thus the gate is heavily doped and exhibits low resistivity. Donor atoms land in the substrate just outside the "shadow" of the gate, and form the two n^+ (heavily doped n) regions indicated as *source* and *drain* in Fig. 1.20; these regions are typically 0.04 to 0.2 μm deep. The heavy doping results in low resistivity for these regions, since the abundance of free electrons in them is available for conduction. Subsequent high-temperature fabrication steps cause a diffusion of the dopant atoms both vertically and laterally. This *lateral diffusion* causes the source and drain regions to extend slightly under the gate as shown in the figure. The resulting overlap distance is typically 0.02 to 0.1 μm.

The region between the source and drain is called the *channel*. The channel *width W* and *length L* of individual transistors can vary greatly (from a fraction of a micrometer to several hundred micrometers), depending on circuit design needs. In digital circuits, L is normally kept at the minimum value possible.

As we will see below, if the gate potential is made sufficiently positive with respect to other parts of the structure, electrons can be attracted directly below the insulator (near the "surface" of the body). These electrons can come through the n^+ regions, where they exist in abundance, and can fill the channel between them; for this reason the device in Fig. 1.20 is referred to as an *n channel* device (the opposite-type device, called *p-channel*, has holes in its channel and will be considered later). The number of electrons in the channel can be varied through the gate potential. This can cause a variation of the "strength" of the connection between the two n^+ regions, resulting in transistor action. If the two n^+ regions are biased at different potentials, the lower-potential n^+ region acts as a source for electrons, which then flow through the

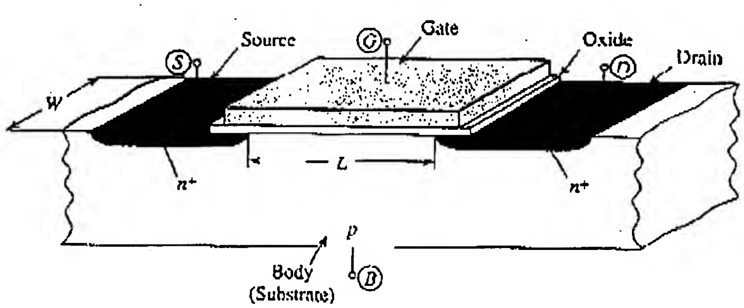

FIGURE 1.20
Simplified structure of an n-channel MOS transistor.